

CLAIMS

1. A conductive line for a semiconductor device including:  
a first conductive layer;  
5 a Titanium layer; and  
a first Titanium rich Titanium Nitride layer between the first conductive layer and the Titanium layer.
2. A conductive line according to claim 1, wherein the first conductive layer is in  
10 direct contact with the first Titanium rich Titanium Nitride layer.
3. A conductive line according to claim 1 or 2, wherein the Titanium layer is in direct contact with the first Titanium rich Titanium Nitride layer.
- 15 4. A conductive line according to any one of the preceding claims, wherein the first conductive layer is a metal layer.
5. A conductive line according to claim 4, wherein the first conductive layer is an aluminium alloy.  
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6. A conductive line according to claim 5, wherein the aluminium alloy is an aluminium copper alloy.
7. A conductive line according to any one of the preceding claims, wherein the  
25 Titanium layer is less than about  $500 \times 10^{-10}\text{m}$  (500 Angstroms) thick.
8. A conductive line according to claim 7, wherein the Titanium layer is from about  $60 - 110 \times 10^{-10}\text{m}$  (60 - 110 Angstroms) thick.
- 30 9. A conductive line according to any one of the preceding claims, wherein the first Titanium rich Titanium Nitride layer is a  $250 - 500 \times 10^{-10}\text{m}$  (250 - 500 Angstroms) layer.
10. A conductive line according to any one of the preceding claims, wherein the first conductive layer is a  $4000 - 8000 \times 10^{-10}\text{m}$  (4000 - 8000 Angstroms) layer.  
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11. A conductive line according to any one of the preceding claims, further comprising a second Titanium rich Titanium Nitride layer, and wherein the first conductive layer is between the first and second Titanium rich Titanium Nitride layers.
- 5 12. A process for manufacturing a conductive line, comprising the steps of:  
depositing a Titanium layer onto a substrate;  
depositing a first Titanium rich Titanium Nitride layer to the other side of said Titanium layer relative to said substrate; and  
depositing a first conductive layer to the other side of said first Titanium rich  
10 Titanium Nitride layer relative to said Titanium layer.
13. A process according to claim 12, wherein the Titanium layer is deposited directly onto said substrate.
- 15 14. A process according to claim 13 or 14, wherein the first Titanium rich Titanium Nitride layer is deposited directly onto said Titanium layer.
15. A process according to claim 13, 14 or 15, wherein the first conductive layer is deposited directly onto said first Titanium rich Titanium Nitride layer.  
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16. A process according to any one of claims 12 to 15, further comprising the step of depositing a second Titanium rich Titanium Nitride layer to the other side of said first conductive layer relative to said first Titanium rich Titanium Nitride layer.
- 25 17. A process according to any one of claims 12 to 16, wherein the first conductive layer is a metal layer.
18. A process according to claim 17, wherein the first conductive layer is an aluminium alloy.  
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19. A process according to claim 18, wherein the aluminium alloy is an aluminium copper alloy.
20. A process according to any one of claims 12 to 19, wherein the Titanium layer is  
35 less than about  $500 \times 10^{-10}$  m (500 Angstroms) thick.

21. A process according to claim 20, wherein the Titanium layer is from about 60 - 110 x 10<sup>-10</sup>m (60 - 110 Angstroms) thick.
22. A process according to any one of claims 12 to 21, wherein the first Titanium rich  
5 Titanium Nitride layer is a 250 – 500 x 10<sup>-10</sup>m (250 - 500 Angstroms) layer.
23. A process according to any one of claims 12 to 22, wherein the first conductive layer is a 4000 – 8000 x 10<sup>-10</sup>m (4000 - 8000 Angstroms) layer.
- 10 24. A silicon substrate having a plurality of conductive lines according to any one of claims 1 to 11 thereon.
25. A semiconductor device including one or more conductive lines according to any one of claims 1 to 11.
- 15 26. A memory including one or more conductive lines according to any one of claims 1 to 11.
- 20 27. An integrated circuit including one or more conductive lines according to any one of claims 1 to 11.